**Simple Goal-Oriented Queries**

Show the wafer-level yield for the last 10 lots.

Highlight any wafers with yield below 90% in the latest lot.

Summarize the top 3 most frequent failing test bins in the past month.

Plot the trend of lot-level yield over the last 6 weeks.

List all wafers that exhibit an edge-ring failure pattern this week.

Identify the test program that contributes the most to die failures in the most recent lot.

Compare parametric test failures vs logical test failures in lot 1234.

Find wafers where over 5% of dies failed in a single soft bin.

Check if the current lot’s yield is within control limits based on historical yield data.

Generate a histogram of a selected E-test measurement across wafers in the latest lot.

**Moderate Goal-Oriented Queries**

Track yield trends across multiple lots and identify any persistent low-performing test bins.

Analyze wafer-level yield variation across different test houses for the same product and test program.

Detect any repeating wafer map patterns among failing wafers in the past four weeks.

Compare the yield distributions between two testers to identify if one consistently underperforms.

Investigate whether voltage-related test measurements are the root cause of recent soft bin increases.

Assess whether wafers with edge-ring fail patterns are linked to specific test handlers or probers.

Identify the test measurement families that most frequently cause failures when overall lot yield drops below 95%.

Determine if there’s a correlation between E-test site variation and the yield drop on recent wafers.

Explore whether lots tested using a specific load board have shown a consistent decline in yield.

Analyze whether wafers with center-fail patterns correspond to specific foundries or manufacturing batches.

**Complex Goal-Oriented Queries**

Analyze all wafers from the last 6 weeks and detect recurring spatial patterns in the wafer maps that correlate with low yield.

Investigate whether yield dips on lot-level over the past two months are associated with any specific test program or family of parametric tests.

Determine whether a consistent low-yield pattern appears only when a specific test house or tester is involved.

Compare the yield distribution across all wafers tested with different load boards and identify if any load board consistently results in lower yield.

Correlate failing die locations with probe touch-down order and detect whether failures align with early or late probing cycles.

Identify whether any logical tests are disproportionately contributing to soft bin counts on lots below the 95% target yield threshold.

Evaluate the temporal correlation between E-test site means and the average parametric values of a particular failing test family.

Find if any significant correlation exists between the test bin distributions and tester configurations (e.g., site count, probe card ID) for failing lots.

Trace the root cause of yield variation within a lot by comparing wafer-to-wafer variation of parametric test measurements.

Detect abnormal grid or checkerboard patterns in wafer maps and determine their association with specific handler or prober settings.

**Multi Goal-Oriented Queries**

For all wafers in the past 2 months with yields below 90%, identify the most frequent test bins, determine if those bins map to a common test program or hardware setup, and suggest if retesting might improve the yield.

Examine all lots from Test House X with yield drops, analyze their wafer-level maps for known patterns (e.g., center, edge-ring), and correlate those patterns to specific test measurement families and E-test values.

Compare the yield of lots tested on Tester A vs. Tester B within the same test house over 3 months, determine if any test measurements are driving the differences, and identify whether calibration differences or load board changes could be the root cause.

Identify test measurements whose parametric limits are frequently causing yield loss across multiple projects, simulate relaxed limits, and estimate potential yield recovery.

Monitor recent lots with yield between 92% and 95%, detect trends in E-test fluctuations, highlight lots with statistically significant wafer-to-wafer parametric variation, and recommend lots for additional inspection.

Analyze wafers showing spatial yield patterns, extract the dominant failure bin, correlate with die coordinates and test program version, and assess if software changes may be introducing probing misalignments.

For project DEF, track weekly yield over 6 months, correlate sudden drops with fab process changes reported by the foundry, and identify which test measurements reflect these process shifts.

Detect if certain PCM parameters predict low FT1 yield, isolate the wafers where this correlation is highest, and recommend changes to either PCM test locations or foundry tuning knobs.

Find all lots with wafer-level yield below 80%, identify common soft bins, correlate with E-test means and scribe test results, and summarize whether the yield loss is front-end or back-end related.

Investigate whether grid-like wafer map failures are consistently observed on specific tester-prober combinations, extract associated test bins and test measurement names, and generate a report suggesting hardware debug actions.